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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

Zoran

Serial No.:	10/686,603
Filed:	October 17, 2003
For:	Apparatus and Method for Damping Vibration in a Machine Tool
Examiner:	Erica E. Cadugan
Art Unit:	3722
Our File:	K8000275US

June 2, 2005

DECLARATION OF DON ZORAN UNDER 37 C.F.R. §1.132

Commissioner of Patents
U.S. Patent and Trademark Office
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314
U.S.A.

Dear Commissioner:

I, DON ZORAN, hereby declare that:

1. I have used and constructed machine tools throughout my career, beginning in 1975. I became a Certified Machine Tools Sales Engineer in July, 2001. I have been

employed in connection with machine tools, both as a tool and die maker, and also in building, servicing and selling machine tools since 1975.

2. I am the inventor of the invention disclosed in the above-identified application and therefore I am familiar with the invention described in the above-identified application and have reviewed the Office Action dated April 13, 2005 together with the reference cited therein. I make this Declaration in support of the arguments to be made in the Applicant's response to the office action which are that Bennett et al. does not teach, suggest or render obvious the invention as presently claimed.

3. A machine tool is defined as follows (Academic Press Dictionary of Science and Technology, 1992):

> Any stationary power-driven machine designed primarily for shaping and sizing metal parts.

As indicated in the Background of the above-identified application, "known machine tools typically produce a great deal of vibration when operating" (para. 0003). When operating, the machine tool is performing a machine tool function, which is defined in the application as including one or more material removal processes (para. 0001). Typical material removal processes which are performed by machine tools are described in paragraph 0001 of the application as follows:

> turning, boring, drilling, reaming, threading, milling, shaping, planing, and broaching.

In order to perform a machine tool function, therefore, the workpiece must be subjected to very high stress, because the workpiece is metal. For example, a typical modulus of elasticity for steel is approximately 30×10^6 psi, and a typical modulus of elasticity for aluminum is about $10\text{-}11 \times 10^6$ psi (Smith, The Science of Engineering Materials (2^{nd} ed.,

1977)). Machine tools typically produce a substantial amount of vibration because of the relatively large amounts of stress to which the workpiece must be subjected in order to remove material therefrom. In addition, and as known in the art, the material removal process must be performed to a relatively high degree of accuracy, notwithstanding the very large stresses to which the workpiece is subjected. For example, a machine tool typically is required to produce a part within 0.001", and can be required to meet a tolerance of as little as 0.0001".

4. The high vibration level which typically accompanies material removal processes in machine tools are undesirable because of three consequences of the vibration:

(a) the tool performing the material removal process is vibrated, adversely affecting the accuracy to which the material removal process is performed;

(b) the vibration resulting from the material removal process causes excessive noise to be generated, affecting the health and safety of the workers; and

(c) the vibration can, ultimately, destroy the machine tool itself.

5. Although the Applicant is a person skilled in the art, it took many years of research to develop a machine tool which would operate with substantially reduced vibration, and a method for making such a machine tool. To do this, the machine tool must have sufficient vibration-reducing capabilities to achieve the desired reduction in vibration but have sufficient stiffness to perform material removal processes within the required tolerances.

6. Bennett et al. is cited in the office action dated April 13, 2005 (at p. 5) as teaching "all aspects of the present invention", except that the constituent parts are made of machined steel. However, Bennett et al. describes a device to be used for chemical mechanical polishing. Chemical mechanical polishing is described in U.S. Patent No. 5,897,426 (Somekh), at col. 1, lines 21-35, as "one accepted method of planarization" used in the manufacture of integrated circuits. Based on a paper (attached) in which chemical mechanical polishing is described, it is my understanding that this process involves downward pressure of about 4-10 psi on a silicon workpiece. Therefore, the stresses to

which a workpiece is subjected in chemical mechanical polishing are very small, unlike the stresses which a machine tool must be able to withstand without affecting accuracy.

7. Bennett et al. thus discloses a solution to a problem which is very different from the problem which the invention herein was invented to address.

8. I have been continuously engaged in the design and manufacture of machine tools since 1975. As a skilled person in the art of machine tool manufacture for 30 years, I note that the need for a machine tool which operates with substantially less vibration has been long recognized. The Applicant's design is estimated to reduce noise levels by about 15% to 20%.

9. As indicated in paragraphs 0004-0005 of the application, the prior art indicates that using monolithic castings to form components of machine tools are preferable, the idea being that vibration is more efficiently dissipated in a larger mass. The prior art thus teaches away from the invention. However, castings have a number of disadvantages when compared to the invention, in which components are made up of machined steel constituent parts with damping material therebetween.

10. Although only recently introduced to the market, the apparatus of the invention has achieved a significant degree of commercial interest. Starting after October 17, 2003, and without advertising (except through one-on-one discussions), five units embodying the Applicant's design herein have been sold.

11. The applicant has provided an economically feasible solution permitting operation of machine tools with much reduced vibration. To my knowledge, there is not another machine tool on the market that can meet the specifications and economic feasibility of machine tools produced by the process and apparatus of the present invention. Applicant's process and apparatus finally provide an inexpensive and reliable solution to resolve a long-felt need, thus providing evidence of the novelty and unobviousness of the presently claimed method.

12. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that wilful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such wilful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed at Cambridge, Ontario and dated this 2nd of June, 2005.

DON ZORAN

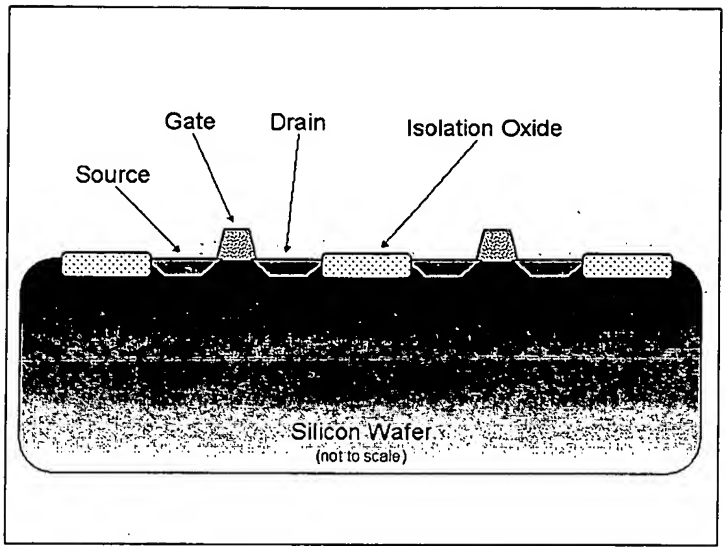
WAT_LAW\1735285\5

Chemical Mechanical Polishing (CMP)

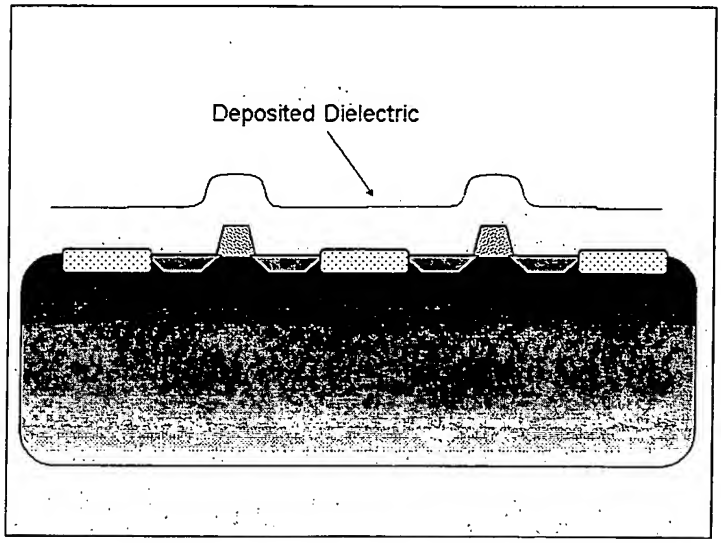
This document is intended to introduce the techniques of Chemical Mechanical Polishing (CMP) to the new user so that they may be better prepared to integrate CMP into their process flow. CMP can be used for many different purposes but it is limited in what it can do and what substrates it can handle. If after reading through this document you still have questions regarding what can be done here at the CNF, please contact the staff member in charge of the tool.

History

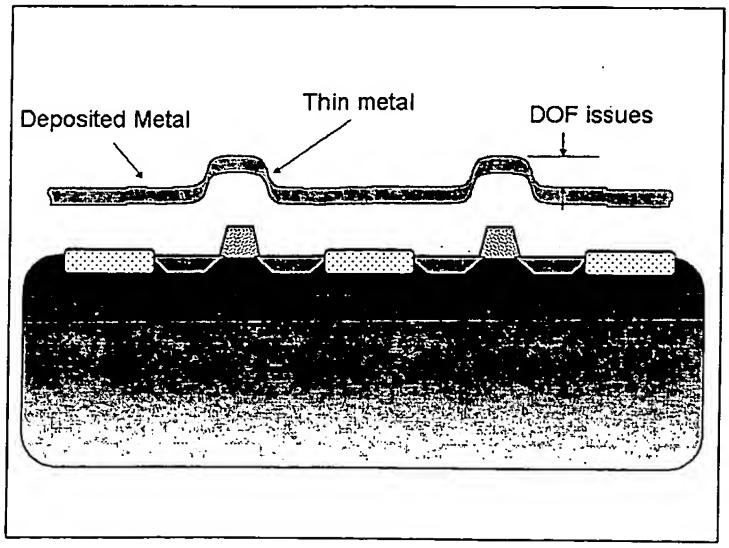
IBM invented CMP in the late 80's to allow for more metal layers in the integrated circuits (IC) that they produced. Originally it was called Chemical Mechanical Planarization (CMP) since that was the purpose for which it was created. A typical transistor wiring process flow of the time is shown.



After creating the transistors in the silicon, a dielectric (typically silicon oxide) was deposited. The deposited material replicates the step height of the underlying surface and in some cases can actually increase the topology. When the metal is deposited to form the first wiring level, the metal thickness can significant thin over the edges of the feature. This causes a reduction in the wire cross-section and a subsequent increase in the wire resistivity.

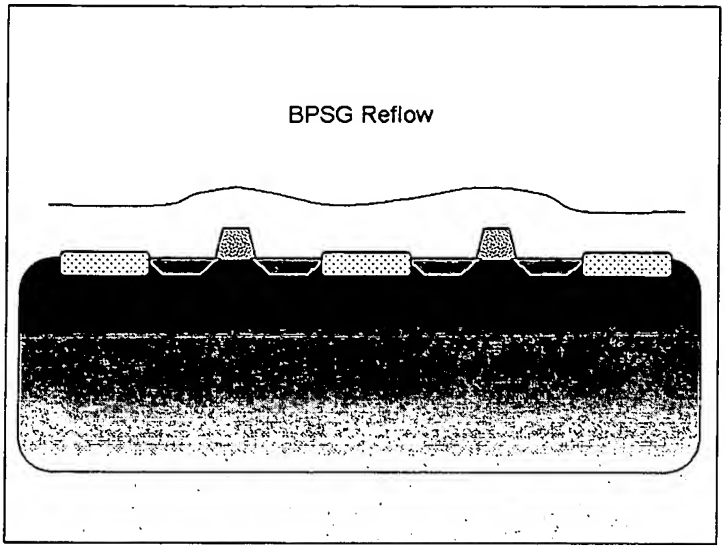


Additionally, the step height causes problems when trying to do high-resolution lithography. Pushing optical lithography tools to print ever-smaller features requires moving toward high numerical aperture (NA) tools. These tools can print smaller features at the expense of a smaller depth-of-focus (DOF) window. This requires that the surface height of the film they are patterning to be within a narrow range for the image to print accurately. Any topology in the surface makes it difficult to focus the image on both the high and low areas.

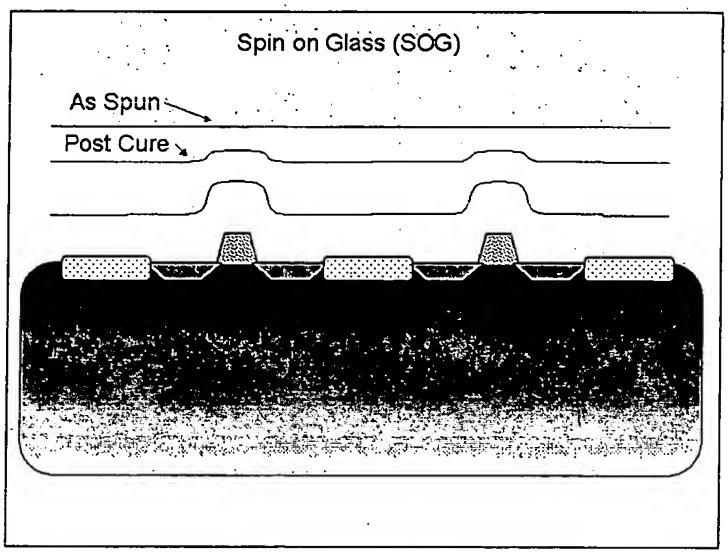


Other Planarization Techniques

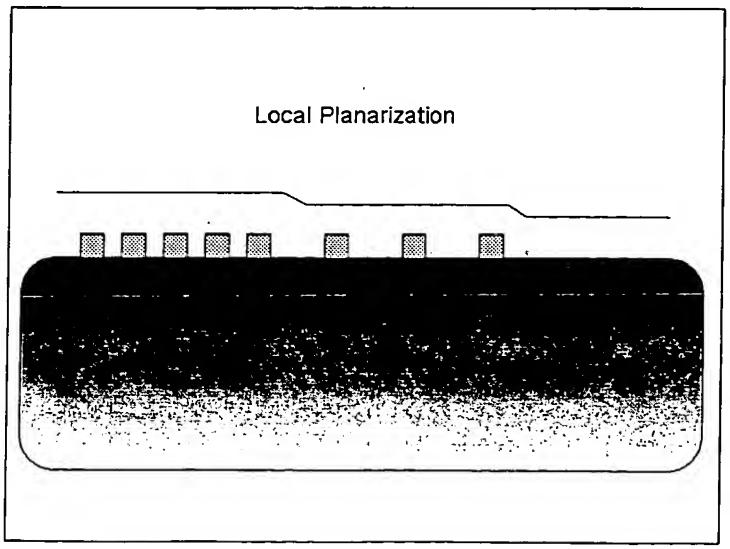
To remove step heights in the dielectric, IC companies used a variety of techniques prior to CMP. One technique was to deposit a silicon oxide layer heavily doped with boron and phosphorus, (Boron-Doped Phosphosilicate Glass-BPSG). This material has a lower melting point than undoped silicon oxide. A high temperature anneal was performed and the material would reflow slightly and smooth out the step heights.



An alternate strategy was to use a Spin on Glass (SOG) material. This is a liquid silicon oxide organic precursor that is spun on the wafer in a manner similar to photoresist. Being liquid, the material planarizes the surface before the solvent is baked off. After it is spun on, the material undergoes a high temperature curing process. During this cure, most of the organic constituents are driven off and the material shrinks to form a type of silicon oxide dielectric. The main issues with this type of process is that the quality of the oxide is very poor compared to a thermal oxide, and it does not completely remove the step height due to differences in the total film shrinkage between thick and thin areas.



Many other techniques were utilized as well but all of them suffered from various drawbacks. The main problem with even the best techniques was that they only achieved local planarization. There was still a height variation between areas of the chips that had different pattern densities. This caused depth of focus problems with the lithography steps.

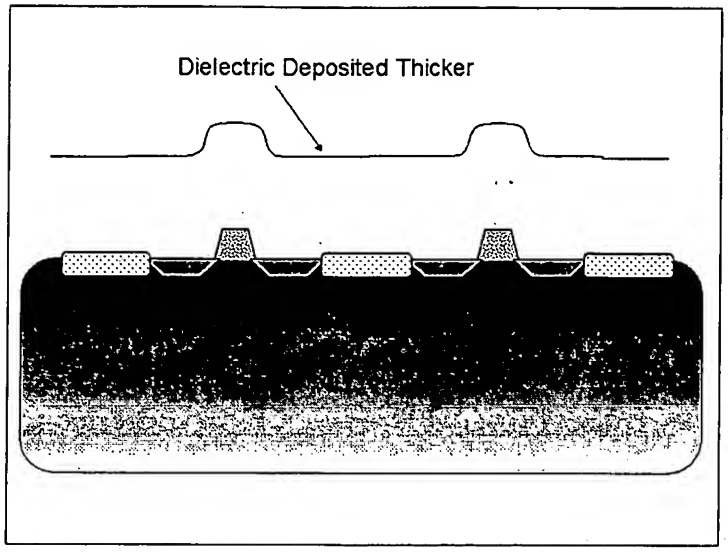


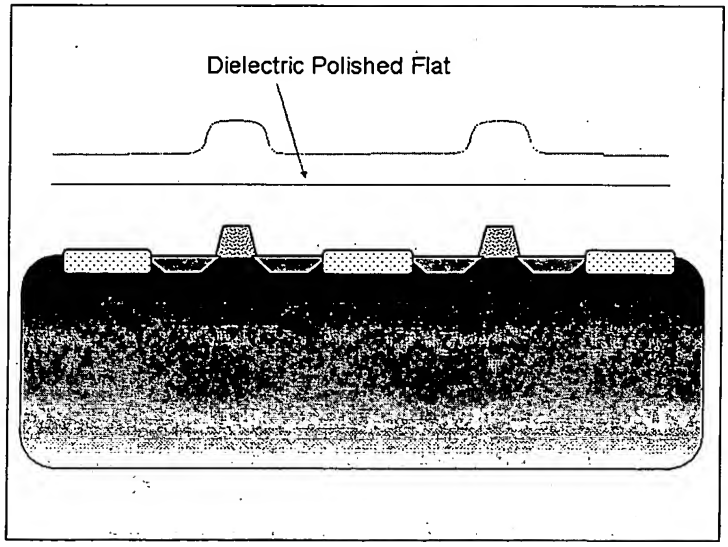
CMP Planarization

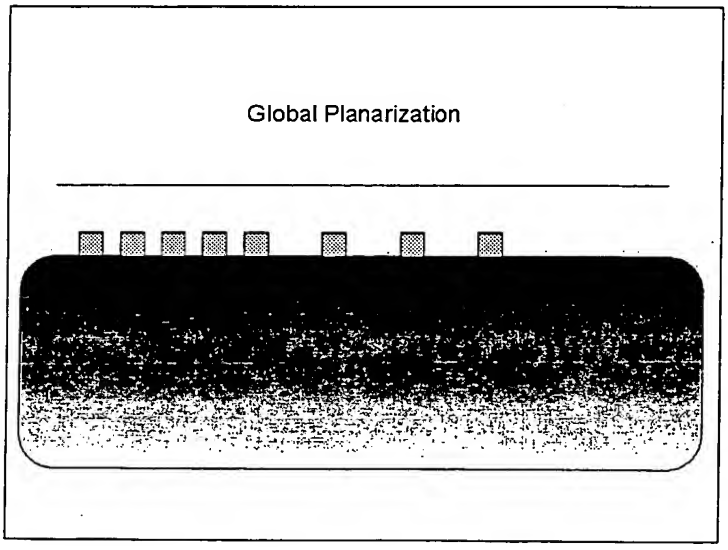
CMP improved on the alternate planarization techniques in many ways. The basic process is to deposit the silicon oxide thicker than the final thickness you want and polish the material back until the step heights are removed. This gives you a good flat surface for the next level. In addition, the process can be repeated for every level of wiring that is added.

CMP is the only technique that performs global planarization of the wafer. This is absolutely required to increase the number of wiring levels in the integrated circuits. Prior to CMP, DOF issues due to global planarization problems limited the total number of IC wiring levels to 3 – 4. With CMP, current state of the art IC production is able to achieve 7 – 8 wiring levels.

These achievements did not come without any cost. Many companies were hesitant to integrate CMP for several different reasons. One is that the process suffers from defect issues due to scratching of the wafer surface and from problems removing the abrasive particles when the polishing is finished. In addition, early CMP suffered from being a bit more of an art than a science. The polishing process was not well understood and variations in the material used to perform the polishing caused process shifts that were hard to correct. As the process has matured, many of those issues have been resolved and CMP is now viewed as a more accepted IC processing technology.



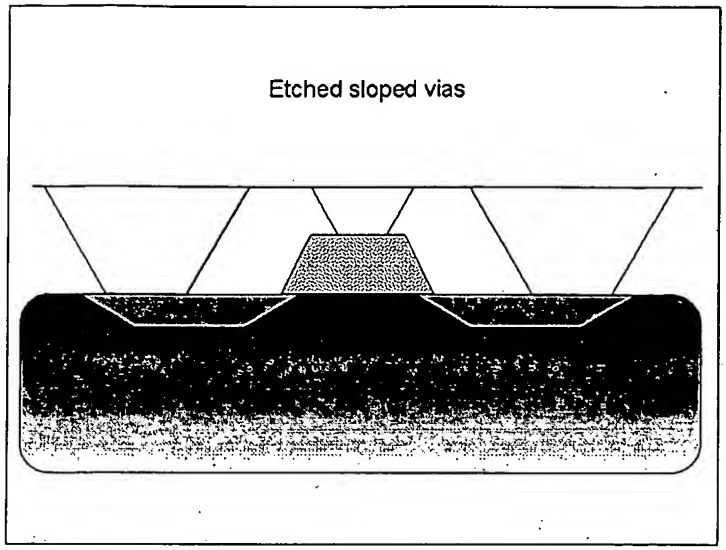


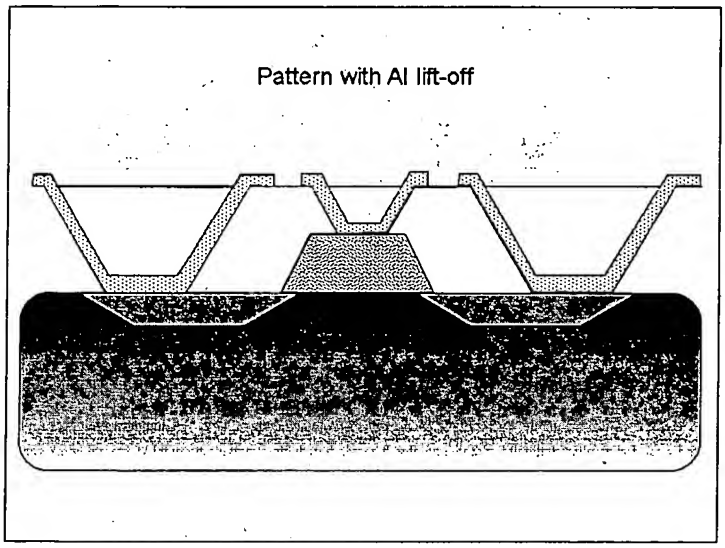


Damascene CMP

An alternate use for the CMP process was for creating inlaid metal patterns on the wafer for the wiring levels. This is called a damascene process. It was used to replace the traditional method of making electrical contacts between the IC wiring levels.

Traditionally to contact the source, drain, and gates of the transistors, large sloped holes or vias were etched into the dielectric, and the wiring metal was patterned over the hole and allowed to contact the lower level directly. The main detractor with this process is the amount of lateral space each contact took up, preventing high-density packing of the transistors.

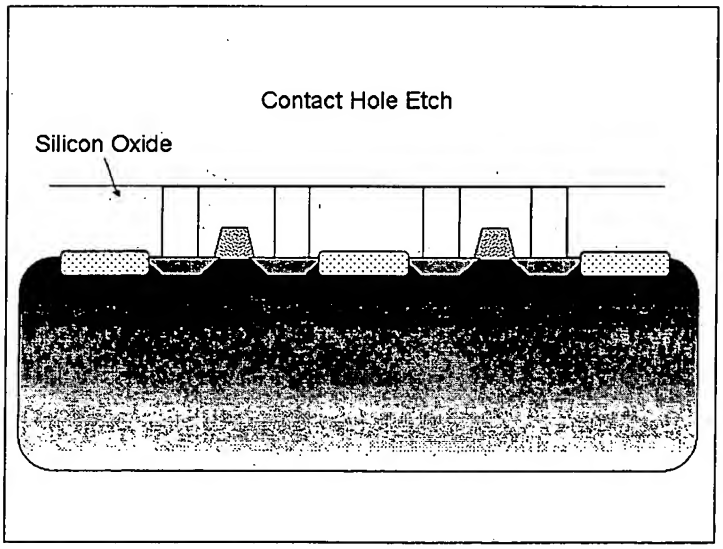


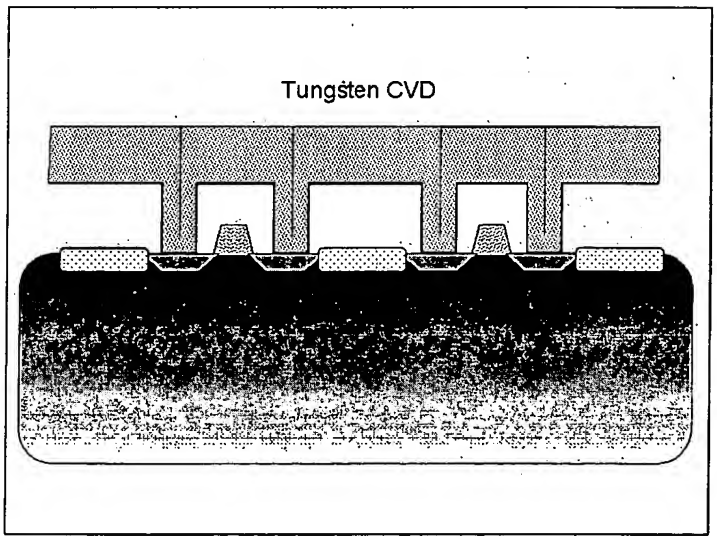


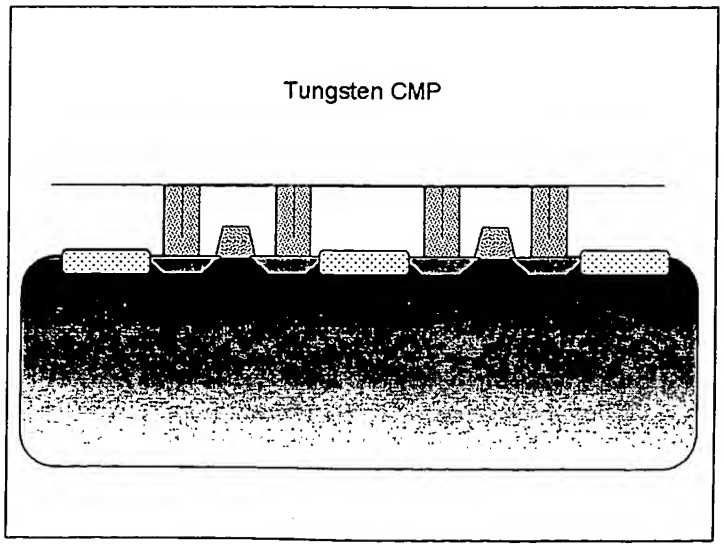
The tungsten damascene process starts with a fully planarized dielectric surface that is patterned with vertical contact holes. These holes can be made much smaller and spaced tighter than the sloped vias of the previous process. Tungsten (W) is then deposited using a chemical vapor deposition process to produce a uniform coating thickness on all exposed parts of the wafer. In this two phase process, the tungsten precursor (WF_6) migrates to the wafer surface where is decomposes into solid tungsten and a volatile by-product. The CVD process 'grows' a crystalline tungsten film that fills the holes from all sides, producing a hole that is completely filled with metal, leaving only a very narrow seam down the middle of the contact hole. Usually a barrier / adhesion layer is put down first (not shown) to reduce electrical resistance to the underlying metal and protect it from the corrosive W CVD chemistry. A CMP process is then

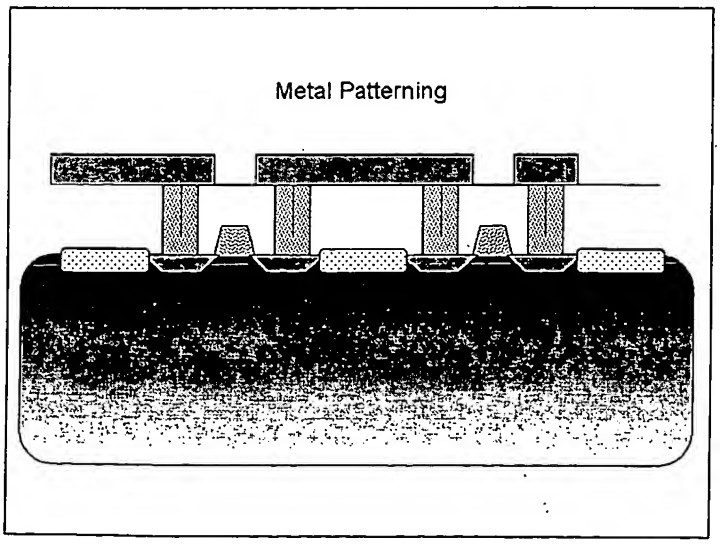
employed to remove the surface tungsten, leaving behind the filled contact holes. This polishing process is designed to be highly selective in removing the tungsten versus the underlying dielectric. This allows the process to use the dielectric as a stopping layer, improving the process latitude. Finally a metal layer is patterned on top of the filled contacts to complete the circuit. This process is repeated with the oxide planarization step to add each wiring level to an IC.

Instead of just being used to pattern vias for connecting two wiring levels, the damascene process can be used with trenches patterned in the dielectric to form the wiring themselves. In this process, a shallow trench is etched in the dielectric in the shape of the desired wire, the metal is deposited on the wafer, and the CMP process selectively removes the material to leave the trench filled. This process is one of the key technologies that has enabled the integration of copper into IC wiring levels. Prior to this, there was no way to easily pattern small copper features since copper cannot be plasma etched. The damascene process is also utilized in the Shallow Trench Isolation (STI) scheme to further permit tighter transistor packing.



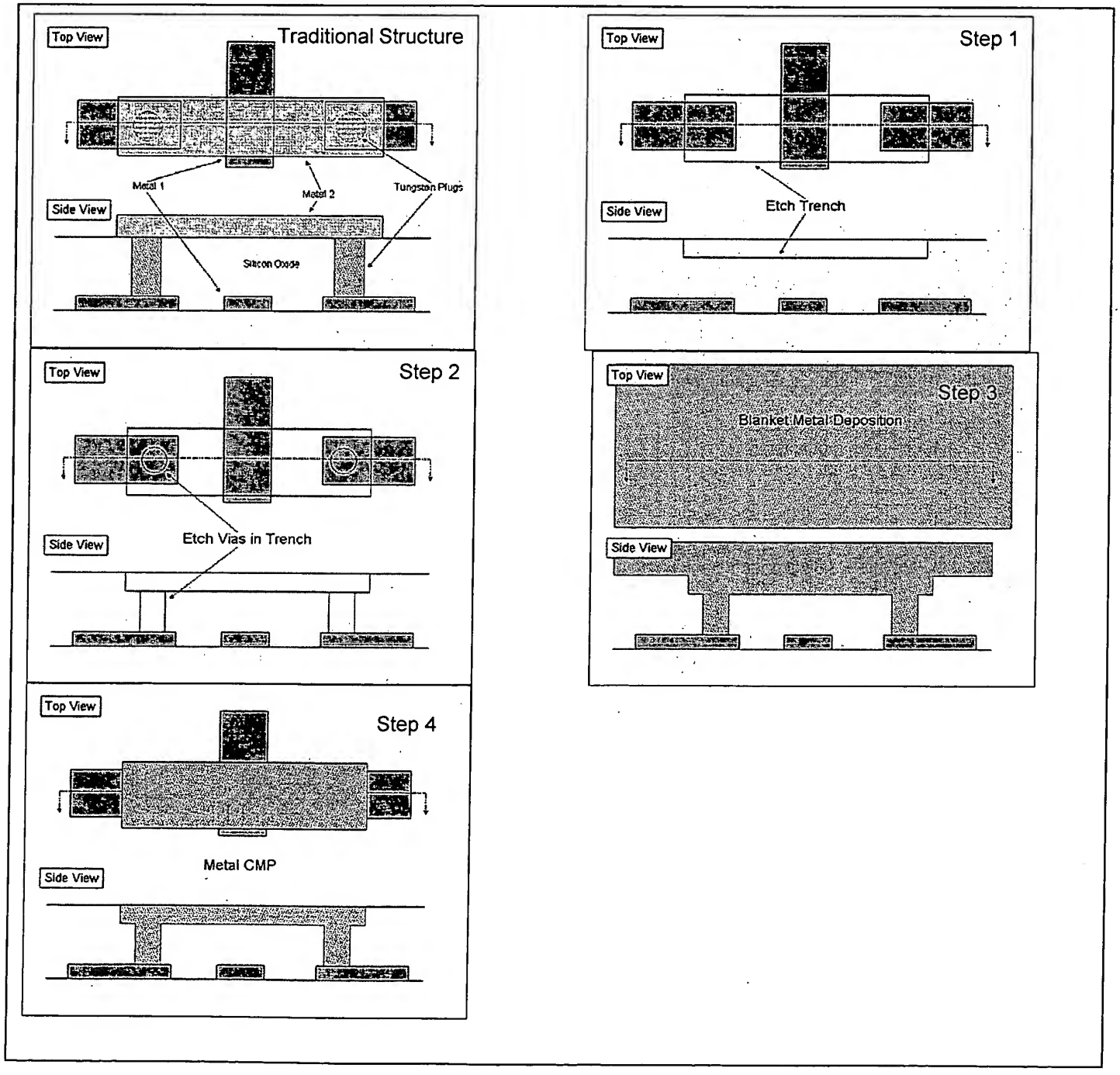






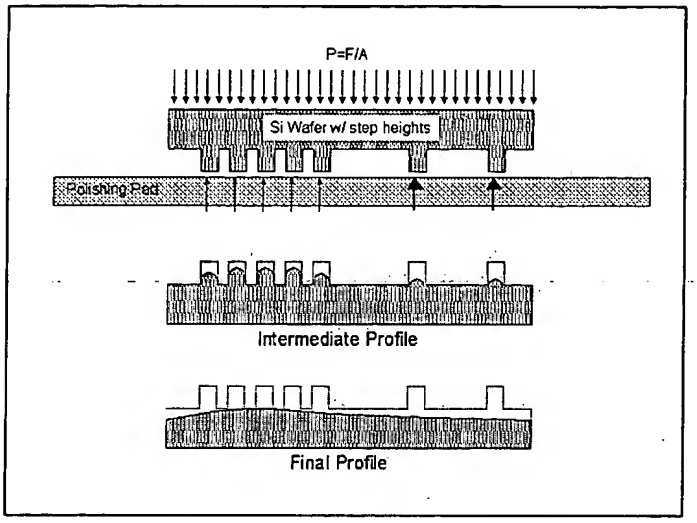
Dual Damascene CMP

In the dual damascene process, both the wiring level and the interlevel connections are created with a single polishing step. Two patterning steps are used to create features of two different depths. Blanket metal is deposited and a single CMP step is used to create the inlaid structure. This is the current process used by many IC companies to integrate copper into their circuits.



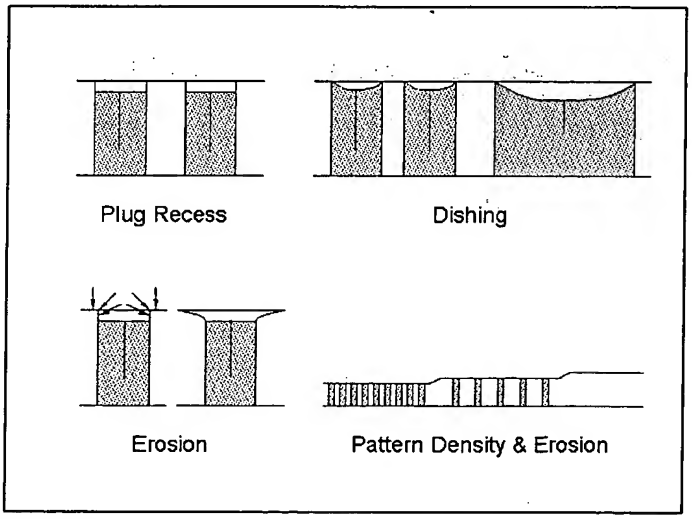
CMP Pattern Density Issues

CMP is seen by most of the semiconductor industry as critical for producing 0.35um devices and smaller, although it does suffer from some problems that need to be accounted for during the process integration. When polishing a wafer that has step features, only the top of the features touch the polishing pad, concentrating the pressure on these contact points. This increases the polishing rate above that of a blanket wafer. In addition, it causes nonuniformity in the removal rate across patterns of different densities due to variations in the pressure distribution across the pattern.



This pattern density effect on removal rate can cause problems if you have very dense and very sparse pattern in your design. Some ways to account for this is to create dummy shapes around the sparse pattern to try and match the higher pattern density.

The damascene process also suffers from several different issues. One issue is that the material being removed usually has a faster etch rate than the material the structure is inlaid in. This can cause two similar problems called plug recess and dishing. Plug recess is where the damascene structure sits slightly lower than the field area due to the faster removal rate than the field. Due to the mechanical limitation on how much the pad can deform, it is usually not excessive. In general, higher chemically active slurries will have a higher amount of recess due to the wet etching action of the slurry.



Dishing occurs when the polishing pad under the pressure of polishing, is able to deform into the damascene structure and polish it below the field area. The amount of dishing that occurs is related to the polishing pad characteristics, the size of the structure, and the polishing parameters (speed, pressure, temperature).

Erosion of the field material can also occur due to the enhanced polishing at the edges of the structures. As the damascene structure gets recessed, the corners of the field area are exposed and erode more rapidly than the unpatterned areas. This affects the local field material polishing rate and can lead to a variation in the field thickness based on the damascene pattern density. The polishing variables can be tuned to reduce this effect but usually at the expense of other parameters (removal rate, uniformity, etc.).

Glossary

Back pressure – During the polishing process, the wafer is held in place on the carrier head by the retaining ring without vacuum assistance. During polishing, air may be blown out the holes in the backing plate to affect the uniformity of the removal rate. This blowing of air is generally measured in pounds per square inch (psi). Nominal values for the back pressure are from 0 – 2 psi. If you set the back pressure too high it will blow the wafer out of the pocket.

Backing film – a cushioning polymer film attached to the backing plate with a pressure sensitive adhesive. It cushions the wafer during the polishing and compensates for slight flatness variations in the wafer or backing plate. The quality of the backing film is important to prevent uneven polishing.

Backing plate – Located in the carrier head, the backing plate is a precision flat stainless steel disk slightly larger than the wafer. It presses against the back of the wafer and transfers the polishing force to the wafer during CMP. Attached to the backing plate between the plate and the wafer is the backing film. There are many small holes in the backing plate to allow the tool to apply vacuum on the back of the wafer to transport it from the load station to the polishing pad. Vacuum is not generally applied during the polishing process.

Brushcleaner – a tool used to clean and dry wafers after CMP.

Carrier head – Tool fixture that holds the wafer against the polishing pad during the polishing operation. The carrier head is specific for the wafer you are polishing. The CNF has carrier heads for 3", 4", and 6" wafers.

CMP – chemical mechanical polishing, or chemical mechanical planarization. Polishing process utilizing both chemical etching and mechanical removal for nanofabrication.

Conditioning profile – varying the pad conditioning parameters over the polishing pad to affect the polishing uniformity. The Strasbaugh 6EC breaks the conditioning arm sweep into 10 zones in which you can set both the conditioning down force and dwell time for each zone.. This allows you to alter the pad characteristics across the wafer track to make improvements in the removal rate uniformity.

Damascene process – CMP process in which a feature is etched in to an already planar film. The features are typically trenches or holes. A second material is then deposited on the wafer filling the feature. The CMP tool is then used to selectively remove the deposited film in the field area, leaving behind the filled feature flush with the planar film.

Diamond disk – a metal disk with embedded industrial diamond particles for conditioning the pad.

Dishing – the thinning of damascene structures below the field area due to pad deformation. Dishing is related to the structure size, pad hardness, and other polishing parameters. See also recess.

Down force – the pressure applied to the wafer during the polishing process. It is expressed in pounds per square inch (psi) with common pressures in CMP being 4 – 10 psi. Below 4 psi the wafer predominantly hydroplanes over the polishing pad and above 10 psi you risk breaking the wafer. The polishing pressure used has a large effect on uniformity and planarization.

Dual damascene – combining etched structures of different heights to fabricate both wiring and interconnects in one damascene polishing process

Erosion – thinning of the field area around damascene structures due to enhanced polishing at the feature edges. The more feature edges you have in a given area, the higher the erosion rate. Erosion issues almost always makes the actual selectivity of a given process lower than that measured on nonpatterned wafers.

Extension – the amount that the top surface of the wafer sits above the retaining ring in the carrier head. If the extension is too low, the etch rate will be reduced on the wafer edge and additionally, the retaining ring will wear down. If the extension is too high the wafer will slip out of the pocket and break during the polishing. Usually measured in mils (thousandths of an inch ≈ 25 microns). The opposite of wafer capture.

Fixed abrasive pads – pads with the abrasive component embedded into it instead of in the slurry. It is used with a chemical only liquid to perform CMP. Recent development in CMP that supposedly gives excellent selectivity.

Microscratching – micro scale scratching caused by debris on the polishing pad, agglomerated slurry particles, and pad defects. These are very hard to prevent from occurring but steps can be taken post polishing to minimize impact.

Pad conditioning – surface treatment of the polishing pad to improve removal rate stability. Hard polishing pads will glaze over from use during polishing and the removal rate will decrease over time. Rubbing the polishing pad with a diamond abrasive disk removes this top glazed surface and uncovers fresh pad material for polishing. Proper conditioning parameters can lead to very stable removal rates.

Planarization – the removal of surface topology in a nanofabricated strucuture. This was original purpose of the CMP process. Planarization can be either just

local removal of step heights, called local planarization, or it can also be uniform removal of material across a die, called global planarization. CMP is currently the only planarization process that gives global planarization.

Polishing pad – a polymer pad that the wafer is rubbed against during the CMP process. It is applied to the polishing table which rotates under the polishing arm. Slurry is dispensed on to the pad and the polishing arm pushes the carrier head against the pad to polish the wafer. Polishing pads are designed with a variety of properties and purposes.

Post-CMP cleaning – CMP slurries contain abrasive particles to perform the mechanical removal of the surface material. These abrasive particles must be removed from the wafer surface after polishing to prevent defects. After CMP, the wafers must be kept wet prior to cleaning because once the slurry is allowed to dry on the wafer, it is very hard to get off mechanically. Due to electrostatic attraction forces though, simply rinsing the wafers with water after polishing will remove little if any of those particles. Modern production equipment use wafer brushcleaners to clean and dry the wafers after CMP. These tools use PVA brushes to mechanical wipe the surface of the wafer and remove the abrasive particles. Additionally, they use dilute ammonium hydroxide to reduce the electrostatic attraction of the slurry particles to the wafer surface. It is important for any CMP process to determine how you are going to clean the wafers when you are done.

PVA – polyvinylalcohol, a soft spongy hydrophilic polymer material used in post-CMP cleaning to mechanically remove slurry particles.

Quill – or Spindle. The motor on the polishing arm that rotates the carrier against the pad. It turns in the same direction as the polishing table.

Removal Rate – the average rate at which material is removed from the surface of the wafer. Most often reported with a uniformity value as measured on a unpatterned wafer.

Retaining ring – a hard polymer ring on the carrier head that surround the wafer when it is mounted on the carrier head. The top surface of the ring sits above the wafer backing plate by a set amount to form a recessed circular area called the pocket. The depth of the pocket is important for successful polishing.

Selectivity – a ratio of removal rates between two different materials for a given CMP process. This is often determined by measuring the average removal rates on blanket film wafers. As an example, for the polysilicon damascene process, the vendor states that the slurry, when used in a specific CMP process, gives a 300:1 selectivity between polysilicon and thermal oxide. The value reported by this method is often much higher than what is achieved on a patterned wafer due to erosion effects.

Shallow Trench Isolation (STI) – Device isolation process for CMOS that utilizes CMP to allow for tighter device spacing. First, a silicon oxide and nitride layer is put down on the wafer to protect the surface from CMP damage. The wafer is etched to leave the device areas raised as 'mesas' with a lower trench area surrounding it. An oxide is deposited over the wafer thick enough to fill the trenches above the height of the mesas. An oxide CMP process is then utilized to remove the oxide over the mesas to expose the active device areas. The silicon nitride layer acts as a stopping layer for the CMP process and protects the silicon from mechanical damage during CMP.

Slurry – a mixture of abrasive and chemicals used to perform CMP. It is continuously pumped on the polishing pad during the CMP process. Most slurries remove material through a combination of chemical and mechanical methods so they are generally material specific. A given slurry may be used to polish materials other than the material it was designed for but unwanted results may occur.

Spindle – or Quill. The motor on the polishing arm that rotates the carrier against the pad. It turns in the same direction as the polishing table.

Surface roughness – a measurement of the surface irregularities. Most often expressed as a root mean square (RMS) value of the height variation in angstroms. A given polishing process will give you a set surface roughness on the small scale, but if measured over large areas it will measure higher due to the microscratching that occurs.

Touch up polish – a quick, low removal polishing step optimized for scratch removal and low surface roughness. Utilized after a primary polishing step to improve the surface finish and reduce defect levels. This type of polish was developed due to the high defect levels from the tungsten damascene process. After the tungsten CMP step, an oxide touch up or buff step would be performed to improve the silicon oxide surface qualities.

Uniformity – a measurement of how uniform the removal rate is across the wafer. It can be measured many ways but the most common is the standard deviation (SD or σ) of the measured removal rate expressed as a percentage of the removal rate. It is also sometimes called a measurement of non-uniformity.

Wafer capture – the amount of the wafer that is in the pocket usually expressed as a percentage of the wafer thickness. The opposite of wafer extension.

SIMTech Technical Report (PT/01/003/JT)

Chemical Mechanical Planarization

Dr Wang Zhengfeng
Dr Yin Ling
Ng Sum Huan
Teo Phaik Luan

(Joining Technology Group, Process Technology Division, 2001)

A*STAR
Singapore Institute
of Manufacturing
Technology

1 BACKGROUND

Chemical Mechanical Planarization (CMP) is a process that can remove topography from silicon oxide, metal and polysilicon surfaces. It is the preferred planarization step utilized in deep sub-micron IC manufacturing. More recent scaling of transistor critical dimension has required the use of CMP for applications such as shallow trench isolation (STI) and trenched metal interconnection (Cu damascene). CMP has also been utilized for fabrication and assembly of Micro Electro-Mechanical System (MEMS).

In principle, CMP is a process of smoothing and planing surfaces with the combination of chemical and mechanical forces. It can, in a way, be thought of as a hybrid of chemical etching and free abrasive polishing. Mechanical grinding alone may theoretically achieve planarization but the surface damage is high as compared to CMP. Chemistry alone, on the other hand, cannot attain planarization because most chemical reactions are isotropic. However, the removal and planarization mechanism is much more complicated than just considering chemical and mechanical effects separately. CMP makes use of the fact that high points on the wafer would be subjected to higher pressures from the pad as compared to lower points, hence, enhancing the removal rates there and achieving planarization.[1]

CMP is most widely utilized in back-end IC manufacturing. In these process technology and steps thin layers of metal and dielectric materials are used in the formation of the electrical interconnections between the active components of a circuit (e.g. transistors, as formed in the front-end processing). As shown in figure 1, the interconnect is manufactured by depositing thin films of materials, and selectively removing or changing the properties of these materials in certain areas. A new level of thin film is deposited on top of old films and the process is repeated many times until the interconnect is complete. The goal of the CMP process is to planarize step heights caused by the deposition of thin films over existing non-planar features, so that further levels may be added onto a flat surface.[2]

Damascene process, as well as its upgraded generation – dual-damascene, is the critical technology in the transition from aluminum to copper interconnects in semiconductor manufacturing.[3] There are two primary factors driving this transition: the lower resistivity and the increased electromigration resistance that copper offers relative to aluminum. Several new materials and processes are required in this change. In the copper interconnect fabrication process, a simpler dielectric etching replaces metal-etch as the critical step that defines the width spacing of the interconnect lines, while the burden of planarization shifts to the metal deposition and CMP steps.

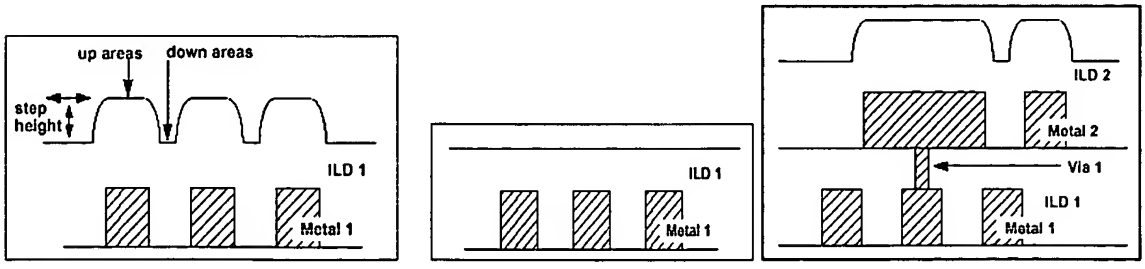


Figure 1 Cross-section diagram of internal dielectric on top of metal line before and after CMP (the left and the middle charts) and application of Metal 2 and ILD 2 (the right chart)

Keywords: Chemical mechanical planarization (CMP); Copper damascenes process; Semiconductor industry; Metrology; Microelectromechanical system (MEMS)

During the CMP of patterned copper wafers, two phenomena – copper dishing and SiO_2 erosion – lead to deviations from the ideal case depicted in figure 2(a). Copper dishing and SiO_2 erosion occur during the over-polish step (which is required to ensure complete copper removal across the entire wafer) and are defined schematically in figure 2(b).[2]

Copper dishing is defined as the difference in height between the center of the copper line – i.e. the lowest point of the dish – and the point where the SiO_2 levels off – i.e. the highest point of the SiO_2. Copper dishing occurs because the polishing pad bends slightly into the recess to remove copper from within the recess. The SiO_2 erosion is a thinning of the SiO_2 layer resulting from the non-zero polish rate of SiO_2 during over-polish step. The SiO_2 erosion is defined as the difference in the SiO_2 thickness before and after the polish step. Both copper dishing and SiO_2 erosion are undesirable because they reduce the final thickness of the copper line; and copper dishing leads to non-planarity of the surface resulting in complications when adding multiple levels of metal.

CMP is also readily adaptable as an enabling technology in Micro-electro-mechanical Systems (MEMS) fabrication, particularly polysilicon surface micromachining.[4] CMP not only eases the design and manufacturability of MEMS devices by eliminating several photolithographic and film issues generated by severe topography, but also enables far greater flexibility with process complexity and associated designs. Thus, the CMP planarization technique alleviates processing problems associated with fabrication of multi-level polysilicon structures, eliminates design constraints linked with non-planar topography, and provides an avenue for integrating different process technologies. Examples of these enhancements include the extension of surface micromachining fabrication to multiple mechanical layers, as illustrated in figure 3, the monolithic integration of electronics and MEMS, and the combination of bulk and surface micromachining.

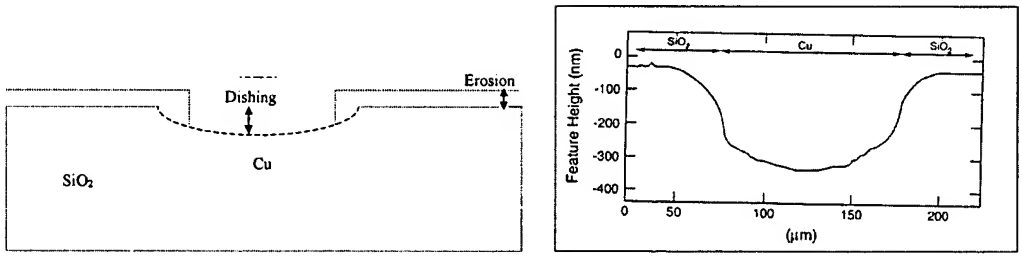


Figure 2 Left chart: (a) Schematic representation of copper dishing and SiO2 erosion; Right chart: (b) Profilometer trace of a 100μm line exhibiting 305nm of dishing

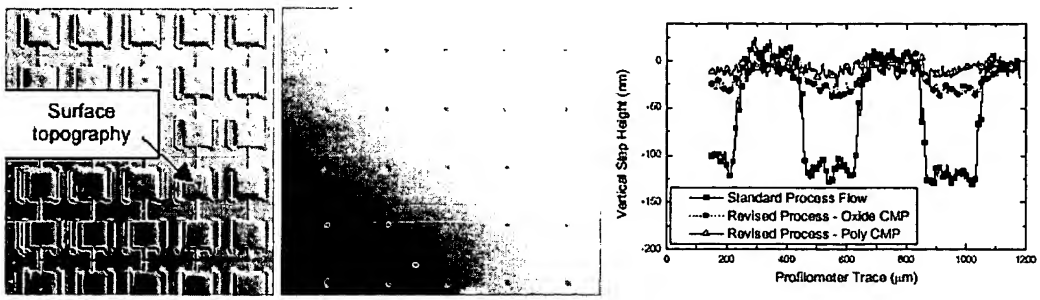


Figure 3 Two SEM images show the surface of polysilicon before and after CMP polishing and the result of profilometer measurement

2 OBJECTIVE

The objective of this project is to build up the capabilities of Gintic in the CMP process. The study of the CMP process of inlaid copper structures was highlighted as the main investigation direction because of the potential of copper as the next generation interconnect material.

3 METHODOLOGY

The design of experiments started with the design of a photolithography mask for the transfer of the etch pattern onto the wafers. The structural layers and fabrication procedure of the patterned wafers were also worked out and sent for fabrication by the Institute of Microelectronics. Schematic cross-sectional view of test wafer is illustrated in figure 4, as well as its SEM images. Copper layer of 2~3μm is desired to fill up the trenches of SiO_2. Adhesion layer under the electroplating metal is 100nm thick.

The geometric design of test wafer is to investigate the dependence of the pattern density and line width versus polishing quality, ie., the dishing in copper connections and the erosion of the surrounding SiO_2. The major features on the mask are lines and square arrays.[5]

The CMP experiments are conducted based on Okamoto™ SPP-600S (as figure 5), which is an one-head machine for 8″ and 6″ wafers and is designed to polish semiconductor materials such as silicon, carbide, ceramics, metals and brittle materials. It consists of slurry supply system, pad surface condition detector, pad surface temperature detector and pad surface condition detector.

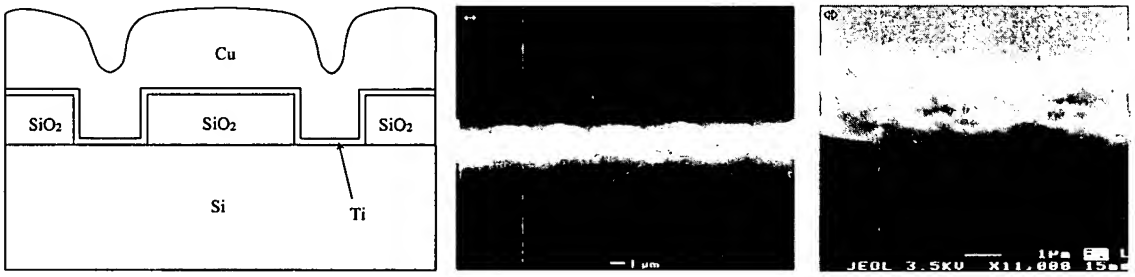


Figure 4 Schematic diagram and SEM images of cross-sectional view of test wafer

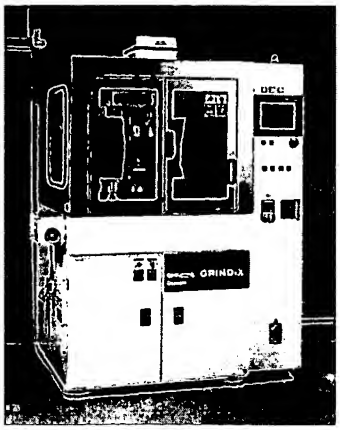


Figure 5 CMP machine

A 2-Phase process is adopted in our inlaid copper pattern wafer polishing, which means changing slurry and working conditions during the copper removal process. The goal of the 1st Phase CMP is to remove copper layer with high efficiency. This phase stops at the surface of the barrier layer. Then changing the slurry and machine status to 2nd Phase for the remaining copper and barrier with removal rate at 1:1 selectivity. The most significant benefit brought by a 2-Phase process is to eliminate the excessive dishing caused by oxidants that is used for high copper removal rate. At the 2nd Phase, lower Cu/barrier selectivity slurry minimizes dishing on patterned structures as well. In order to find out the average efficiency of the 1st Phase removal sequence, the thickness of the copper layer is measured after each fixed process time.

CMP polishing has been performed on the patterned wafers under different head load and speed in order to characterize the polishing quality and process parameters. The surface profiles before and after CMP are fetched through profilometer and atomic force microscopy (AFM) measurement. Some CMP investigations related to the process are also conducted, e.g. polishing pad wearing and SiO_2 polishing.

Gold bump planarization was conducted to explore the application of CMP into electronic packaging. The purpose is to polish the top surface of gold bumps on the silicon wafer and therefore, reduce the surface roughness of bumps in order to enhance the wafer-bumping reliability. The experiment was conducted on a 6″ wafer with arrays of gold bump, which was electroplated on passivation layer for protection of underlying IC.

4 RESULTS

A database has been established that consists of information on the dependence among CMP process parameters, geometrical characteristic of test wafer and polishing qualities on wafer surface. Figure 6 shows the relations between dishing (copper) & erosion (silicon oxide) and pattern characters (pattern density and linewidth). The data are collected from the same wafer and measured by profilometer (>10μm lines) and AFM (<10μm lines) due to the limited scanning scope of AFM (100μm in this case).

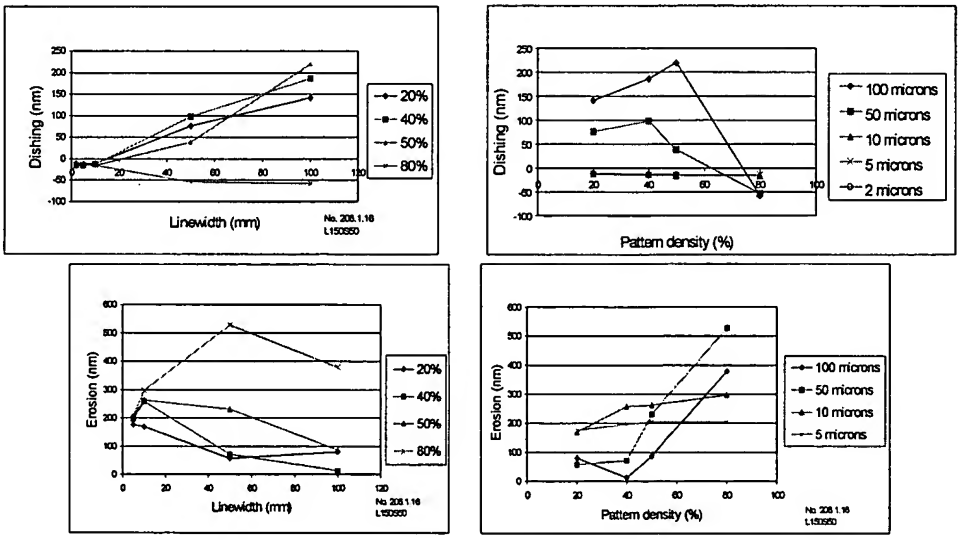


Figure 6 Pattern characters (pattern density & linewidth) versus dishing (Cu) & erosion (SiO_2). 200g/cm^2 of head load and 50rpm of spindle/carrier speed is set for 2nd Phase polishing

By changing the process parameters (head load and spindle/carrier speed), a variety of experiments are conducted and from which, measurements have been taken. By and large, some trends about the relations between process conditions and surface finishing could be extracted as below:

- The severest over-polishing of copper material (dishing effect) normally emerges when the head pressure is about 150g/cm^2 within our experimental scope.
- The dishing depth of copper layer keeps pretty consistent along with the changing of machine speed, while relatively serious over-polishing of copper could be expected when the speed is around 75rpm.
- No obvious trend has been found between the erosion depth of the dielectric layer with the head pressure within our probed process range.
- The most serious over-polishing effect of silicon oxide layer often occurs when the machine speed is around 75rpm.

By analyzing the polishing results from AFM measurement towards copper lines with <10μm width, a common cross-sectional profile, as shown in figure 7, is acquired. From a macro view, over-polishing of copper (dishing) always occurred as illustrated in figure 2, as all the profilometer measurement shows. On the other hand, when lines go to less than 10μm wide, extruding copper lines above the dielectric layer are dominating the situation. One possible explanation for this anomaly is galvanic corrosion between the thin layer of titanium and the copper features. The galvanic corrosion attack occurs from the point when the titanium is first exposed and continues until all the titanium is being removed. It can be said that dishing is occurring in the titanium layer rather than the copper layer.

Gold bump polishing is carried out under typical process conditions. The results indicated in figure 8 show the before and after CMP images on bump surface, which roughness was reduced from 216.00nm to 93.95nm before and after 5 minutes of polishing.

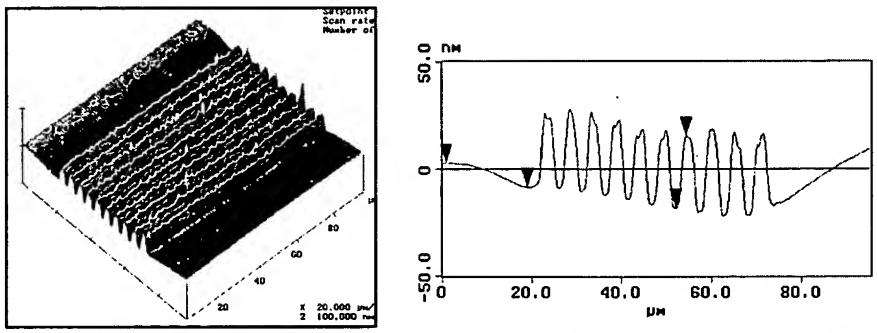


Figure 7 3-D AFM image and section analysis of 2μm copper lines with pattern density of 50%

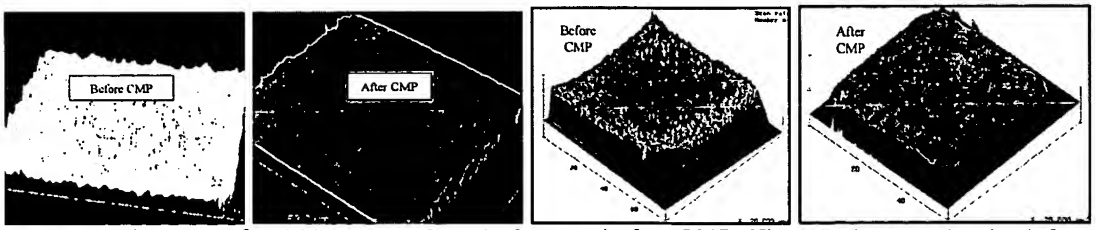


Figure 8 The images of gold bump surface before and after CMP. The two images by the left were taken from Veeco™ laser interferometer and the two by the right from AFM

Within-wafer uniformity of copper polishing is read out as well by taking comparison of dishing heights on copper lines of different dies within the same wafer. An encouraging uniformity of <10% deviation has been acquired in this test.

5 CONCLUSIONS

A variety of CMP experiments of metallic and nonmetallic materials have been conducted. By highlighting on the patterned copper polishing, some trends have been extracted to describe the relations between CMP process conditions and the surface finishing. The promising results on gold bump polishing indicated that the CMP might find its position in electronics packaging applications.

6 INDUSTRY SIGNIFICANCE

CMP plays significant roles in today and tomorrow's semiconductor industry, especially in forming the copper interconnection on silicon wafers. Since the nonstop trend of miniature in device features makes the conventional interconnection technology insufficient to cope with the tremendous pattern density and small line width, copper has been put front as the ideal replacement of conduct material. CMP is the key step to pattern the copper interconnection layer, instead of the conventional etching process that does not work on copper material.

During our project the two crucial defects of copper CMP technology, dishing of copper and over-polish of dielectric, have been investigated. Relevant collaborative researches can be conducted with local and international semiconductor factories, CMP equipment producers and also the consumable (slurry and polishing pad) manufacturers. The possible collaboration fields could be process study on copper polishing and dielectric isolation, consumable development, etc.

More potential applications of CMP can be expected in the field of microelectronics packaging due to the outstanding characteristics of CMP process on surface planarization of various materials and substrates.

Micro-Electro-Mechanical System (MEMS) is an emerging technology that has large potential market value. Apart from the great success in automotive industry by integrating micro sensors with airbag system, Opto-MEMS and Bio-MEMS will be the next two possible areas of large commercial potential for MEMS to explore. CMP can be the ideal tool of surface polishing in the Opto-MEMS and Bio-MEMS packaging, assembly and even fabrication. Along with the growing of MEMS industry, extensive applications of CMP could be explored in these fields.

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Isolation Materials

The high internal damping of the ISODAMP® vinyl and ISOLOSS® urethane material families reduces mechanically or acoustically induced vibrations and dissipates shock and impact energy at a very rapid rate.

These properties—in conjunction with excellent physical strength, flexibility, and good environmental and flame resistance—make E-A-R isolation materials ideal for constrained layer damping, damped isolation and impact control applications.

- Highly effective damped isolation materials for source control of noise, vibration and shock
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- Flame resistant, with excellent wear and physical properties
- Control unwanted motion and rebound in equipment of all types
- Low rebound properties—prevent additive effects of successive impacts
- Available in many forms—sheets, rolls, die-cut and custom-molded parts
- Ideal for high-performance damping in demanding applications such as aircraft, mining equipment, off-road vehicles, ships and military vehicles
- Perfect for do-it-yourself vibration and shock mounts for plant and process equipment

Typical Properties

Property	ISODAMP C-1002	ISODAMP C-1105	ISODAMP C-1100	ISOLOSS HD	ISOLOSS VL
Description	Vinyl Solid	Vinyl Solid	Vinyl Solid	Urethane Solid	Urethane Solid
Hardness Nominal ASTM D2240 15 sec post impact at 23C (73F)					
Shore A Durometer	56	63	70	58	24
Shore OO					70
Flammability UL 94 0.15 cm (0.06 in) thick	Listed V-0	Listed V-0	Listed V-0	Listed HB	Listed V-0
FAR 25.853 (a) Appendix F Part I (a) (1) (12 sec)	Meets at 0.080 cm (0.030 in)				
FAR 25.853 (b-3)	Meets at 0.040 cm (0.015 in)				
MVSS-302	Meets at 0.040 cm (0.015 in)	Meets at 0.152 cm (0.060 in)	Meets at .152 cm (0.060 in)	Meets at 0.32 cm (0.125 in)	Meets at 0.32 cm (0.125 in)
Dynamic Properties ASTM D5279 at 10 Hz, 0.3% Amplitude					
Glass Transition Temperature	-17C (1F)	-13C (9F)	-2C (36F)	-8C (18F)	-34C (-29F)
Max Loss Factor at 10 Hz	.93 at 8C (46F)	.93 at 17C (63F)	.79 at 25C (77F)	0.94 at 12C (54F)	1.20 at -14C (7F)
Compression Set (%) ASTM D395 Method B					
22 hr at 22C (72F)	14	23	24	4.5	4.5
22 hr at 70C (158F), *50C(122F)	62	51	55	6.1	13.3*
Compression Load Deflection kPa (psi) ASTM D575 at 0.51 cm/min (0.2 in/min)					
10% kPa (psi)	490 (71)	634 (92)	1069 (155)	565 (82)	110 (16)
20% kPa (psi)	1682 (244)	2206 (320)	3413 (495)	1241 (180)	152 (22)
30% kPa (psi)	3682 (534)	4785 (694)	7122 (1033)	2103 (305)	193 (28)
Compression Modulus kPa (psi)	5805 (842)	7514 (1090)	1267 (1838)	5826 (845)	945 (137)
Tensile Strength kPa (psi) ASTM D638 51cm/min (20 in/min) at 22C (72F)	10852 (1574)	12459 (1807)	14190 (2058)	8963 (1300)	1765 (256)
Tear Strength kN/m (lbf/in) ASTM D624	35 (202)	42 (241)	53 (305)	38 (218)	49 (280)
Temperature Range C (F) Peak Performance	13C to 41C (55F to 105F)	27C to 54C (80F to 130F)	35C to 63C (95F to 145F)	13C to 41C (55F to 105F)	0C to 32C (32F to 90F)
Recommended Max. Intermittent	82C (180F)	82C (180F)	82C (180F)	107C (225F)	49C (120F)

The data listed in this materials summary are typical or average values based on tests conducted by independent laboratories or by the manufacturer. They are indicative only of the results obtained in such tests and should not be considered as guaranteed maximums or minimums. Materials must be tested under actual service to determine their suitability for a particular purpose.

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RPVC Rigid Polyvinyl Chloride

LEGEND: A = amorphous - Cr = crystalline - C = clear - E = excellent - G = good - P = poor - O = opaque - T = translucent - R = Rockwell - S = Shore

STRUCTURE	A
SPECIFIC DENSITY	1.35
WATER ABSORBTION RATE (%)	0.2
ELONGATION (%)	20
TENSILE STRENGTH (psi)	6500
COMPRESSION STRENGTH (psi)	11000
FLEXURAL STRENGTH (psi)	12100
FLEXURAL MODULUS (psi)	400000
IMPACT (IZOD ft. lbs/in)	5
HARDNESS	R105

FABRICATION

- - BONDING: G

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- - MACHINING: G

DEFLECTION TEMPERATURE (deg. F)

- - @ 66 psi: 170
- - @ 264 psi: 162

UTILZATION TEMPERATURE (deg. F)

- - min: 14
- - max: 40

MELTING POINT (deg. F)	176
COEFFICIENT OF EXPANSION	0.000045
ARC RESISTANCE	70
DIELECTRIC STRENGTH (kV/mm)	18
TRANSPARENCY	C
UV RESISTANCE	G

CHEMICAL RESISTANCE

- - ACIDS: P
- - ALKALIS: E
- - SOLVENTS: G

Plastic Datasheet

ABS Acrylonitrile Butadiene Styrene
CP Cellulose Acetate Propionate
CPVC Chlorinated Polyvinyl Chloride
EVA Ethylene Vinyl Acetate
HDPE High Density Polyethylene
HIPS High Impact Polystyrene
HMWHDPE High Molecular Weight HDPE
In Ionomers (Surlyn)
PAEK Polyaryletherketone
PAS Polyarylsulfone
PB Polybutylene
PBT Polybutylene Terephtalate
PC Polycarbonate
PC/ABS Polycarbonate/ABS Alloy
PEEK Polyetheretherketone
PEI Polyetherimide
PEKEKK
Polyetherketoneetherketoneketone
PES Polyethersulfone
PPE Phenylene Ether Copolymer
PP/Glass f Polypropylene 30% Glass Filled
PPS Polyphenylene Sulfide
PP/Talc Polypropylene 40% Talc Filled
PSO Polysulfone
PUR olyurethane Plastic Rigid
PVDC Polyvinylidene Chloride
PVDF Polyvinyldene Fluoride
RPVC Rigid Polyvinyl Chloride

- Plastic Blending Machinery
- Blow Molding Machines
- Extruding Machines
- Plastic Compounding Equipment
- Plastic Cutting Machines

view all **Processing Equipment**

Plastic Supplies & Raw Materials

- Molding Compounds
- Abrasives
- Inserts for Plastic
- Plastic Additives

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Resins & Compounds

- ABS: Acrylonitrile-Butadiene-Styrene
- CA: Cellulose Acetate
- EP: Epoxy
- EPS: Polystyrene-Expandable
- FRP: Fibreglass Reinforced Plastics

view all **Resins & Compounds**

Plastic Scrap

Thermoplastic Materials

Thermoset Materials

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Chapter 1

Introduction to Chemical Mechanical Polishing (CMP)

1.1 IC Metallization Trends

As we know, the critical dimensions of device and interconnect features on an IC are decreasing while the average wire length between devices is increasing due to increase in die size as shown in Figure 1.1. This simultaneous shrink of features and increase in die area makes for a doubling of IC size every 18 months according to " Moore's Law " or " The Law of the Sand ".

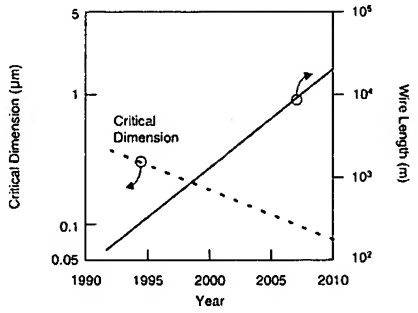

Figure 1.1: Shrinking critical dimension of the devices but increasing wire length.

This situation means that modern IC design for 10^6–10^8 transistors/die is done under the assumption that transistors are free and interconnect delay is costly. Processed and packaged die cost only \$5-50/cm^2 to fabricate while design, verifica-

tion and testing of the same IC is 10× more costly. The next several generations of chips will employ this philosophy which started with the 0.35 micron feature size transistor with 64M transistors in a 2 cm^2 area chip. The average device cell size is 1.3 microns square and the average interconnect is 5 microns long. The next generation 256 M transistor chip with 0.15 micron feature size has a cell area below 1 micron squared and die size of 4 cm^2. Circuit layout process area savings such as stacked or trench memory cell design and trench isolation respectively reduce cell size even further. Still the average interconnect length increases only to 10 microns with 0.15 micron feature size. However, critical path interconnects such as for clocks may approach a large fraction of die size of 1–10 mm.

As a result is the old " simple " two-level metal wiring structure of Figure 1.2 has now evolved into a 5-6 levels of metal wiring. This looks from an IC perspective like a " high-rise " of alternate layers of metal and insulator.

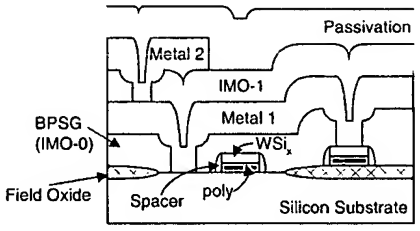

Figure 1.2: Relatively simple two level wiring structure of past IC's.

Surface non-planarity in an IC is cumulative starting from the original flat Si wafer. This is caused by both non-uniform film thickness across the wafer and by the patterned topology of IC features like gates or wiring. As we go up in the upper stories of " high-rise " metalization structures, the metal wire height increases because high current power supply and ground busses are placed in the top layers whereas low current signal busses are placed in the lower level metal layers, as shown in Figure 1.3. To avoid electromigration failure of wires we must keep $J < J_{(\text{critical})}$. Hence, if the current I increases, then wire cross-sectional area A must also increase.

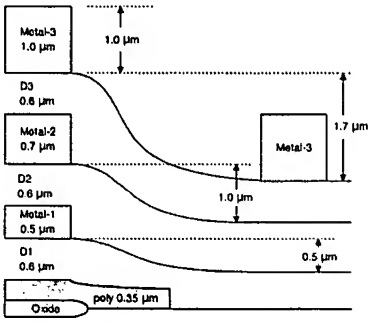

Figure 1.3: Non-planar topology of multi-level wiring structures. For Metal-1, the depth variation for vias may be $\pm 1/2$ micron but for metal three or five this depth disparity may reach +1.5 microns in a non-planarized structure. This non-planar topology makes both etching and uniform filling of all vias in the inter-metal dielectric more difficult. Finally, at some level of non-planarity, both via etching and via filling become impossible to achieve with high yield.

1.2 Problems Arising from Non-Planar Topography

1.2.1 Photo-Printing Difficulties

The ever more non-planar topology as we go into higher metal levels creates problems for photo-printing of desired x-y images in photoresist placed on this rugged terrain. Planarity of $\pm 1/2$ micron is required over 10–20 mm distances of a typical die as we optically print patterns one die at a time using step and repeat cameras of given numerical aperture (NA). These cameras print 10:1 reductions of mask patterns on the wafer. The minimum feature size printed, w, has an associated depth of focus (DOF). As the minimum focus dimension, w, of an optical system is decreased, the DOF of this minimum focus dimension is decreased even more as shown in Figure 1.4. Note that decreasing the camera's NA, while printing finer features, does so with a smaller DOF. The depth of focus budget diminishes greatly with increasing NA.

Including photoresist exposure and development parameters K_1 and K_2, we find:

$$\text{Minimum Resolution} = K_1 \lambda / (NA) = w$$

$$\text{DOF} = \pm K_2 \lambda / (NA)^2$$

Unless truly planar surfaces are presented to the optical tools, the yield of op-

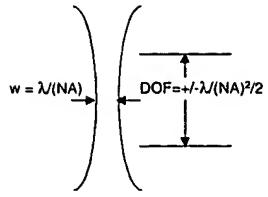

Figure 1.4: Depth of focus (DOF) and minimum focus diminsion.

erating IC's will plummet because patterns with different dimensions w will be printed due to DOF variations of the underlying topology. For example, if gate lengths and widths vary in an uncontrolled manner then gm of transistors will vary also. As a consequence, as designed gate logic may not operate properly. This pattern size variation also gives rise to a variety of defects, lowers IC yields, and reduces profits.

One clear solution to the optical camera dilemma is to planarize each non-planar underlayer to provide a more level topology. We do this for each dielectric layer we just finished making, prior to etching contacts/vias and prior to depositing the next metal layer. In other words, planarize as you work, to better allow submicron photolithography tools to print patterns all the same size.

1.2.2 Difficulty of Both Etching and Filling Vias of Varying Depth

Shown in Figure 1.5 is the varying depth of etch vias through dielectric in between Metal-1 and Metal-2 due to the non-planarity of the underlying PSG (glass) that electrically insulates polysilicon from Metal-1. Note that polysilicon on field oxide lies in a different vertical plane than polysilicon over gate oxide. The PSG glass topology is the foundation or underlayer for Metal-1, and if non-uniform in its vertical topology, puts Metal-1 layers at different heights depending on feature location on the die, which in turn makes etch hole via depths in the dielectric level 1 vary with non-uniform thickness PSG underlayers. Uniform via etching through the dielectric between Metal-1 and polysilicon is impossible, and consequently overetches are a must in order to open all deep vias from Metal-1 to polysilicon as shown in Figure 1.5. The same problem occurs for Metal-2 to Metal-1. However, for all higher metal layers, the planarization of PECVD SiO_2 assists via and metal dimension uniformity.

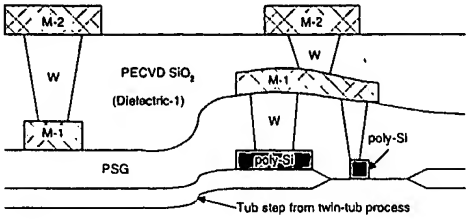

Figure 1.5: Partial planarization of PECVD SiO_2 is a compromise between added fabrication cost and ease of metalization in this illustrative example.

The message is that partial planarization, while helping all photolithography after it occurs, makes via etching and filling to underlayers harder.

Partial planarization solutions are shown in Figure 1.6 where at first we decide the non-planarity of the LOCOS oxide layer is allowed because of the increased cost to remove it, but all higher level oxide layers are planarized by unspecified means. Note the uniformity of Metal-2 to Metal-1 vias made of tungsten, achieved by planarizing PSG alone.

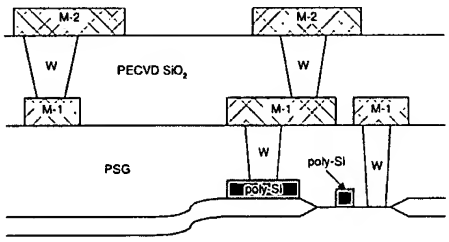

Figure 1.6: Overetching is required to fully open vias of differing depths in different dielectric levels.

By planarizing the top of PSG, the uniformity of vias to substrate is still poor since Metal-1 to substrate or polysilicon vias are of uneven depth, but the Metal-2 to Metal-1 vias are more uniform to both the oxide etch and metal fill processes. Clearly by using trench etching and oxide filling we could also eliminate the non-planarity of the LOCOS topology. This would also allow Metal-1 to either substrate or polysilicon vias to be more uniform. The questions always asked are, "Do the extra steps to achieve planarity increase the IC yield enough to pay back the extra effort cost and time? Does the change even make money by increases in

yield or reliability?"

Partial planarization is not as desirable as full planarization. We need to planarize the underlying dielectric or the metal layers first before we move on to other insurmountable problems. In Figure 1.6 the degree of dielectric planarization is quantified in terms of the two parameters, R and θ. We will use this as a metric to compare various planarization methods throughout this lecture. Good planarity means R is big and θ is small. See Figure 1.17.

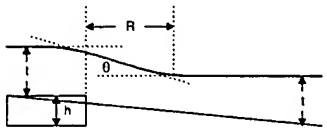

Figure 1.7: Quantitative definition of planarization: R = the relaxation distance, θ = planarization angle.

1.2.3 Full Planarization is Best

Just to anticipate what we can achieve by proper planarization, see Figure 1.8, which shows SEM micrographs of planarization levels before and after CMP of a TEOS oxide layer. Remember that flat is beautiful because photo-lithography, etch, and metalization operate with higher yield.

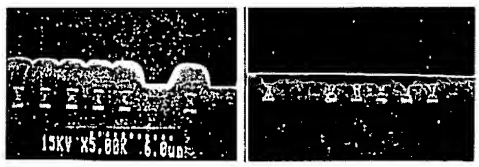

Figure 1.8: SEM photos of a surface planarized using CMP.

There are clearly six extra metal steps for creating via plugs, extra planarization cost and extra lithography steps as shown in Table 1.1 compared to simple processes without planarization. Again, do you pay early for added CMP steps or pay later with lower yield?

Table 1.1: Processing complexity of various multilevel metal structures. All told there are typically 15 steps added to achieve planar topology with W plugs compared to simple Al plugs.

Structure	Process	Dielectric deposition	Metal deposition	RIE or planarization	Lithography	Total
Simple Al non-plug	ILD deposition	2	0	1	0	3
	ILD planarization	0	0	1	0	1
	Via pattern	0	0	1	1	2
	Metal deposition	0	1	0	0	1
	Metal pattern	0	0	1	1	2
	Total	2	1	4	2	9
Full plug layered metal	ILD deposition	2	0	1	0	3
	ILD planarization	0	0	1	0	1
	Via pattern	0	0	1	1	2
	Plug (barrier + W CVD + etch)	0	3	1	0	4
	Metal deposition	0	3	0	0	3
	Metal pattern	0	0	1	1	2
	Total	2	6	5	2	15

1.3 Chemical/Mechanical Polish

Traditionally thick spin on glass (SOG) was employed to planarize non-planar topology. The spin-on process of a thick SOG self-planarized the topology, even if the underlayer was not planar. Excess SOG was traditionally removed by a plasma etchback that did not achieve the desired level of planarity either on a local (10 μm average wire path) or a global (1–10 mm die size) level as shown in Table 1.2 below compared to chemical mechanical polishing (CMP). CMP is an old wet slurry technology borrowed from the optics and disc head business of "lap and polish" as we will describe below.

1.3.1 General

In glass optics, folks have long used such CMP methods to create very flat glass surfaces for precision mirrors, lenses, etc. Over several hundred years an array of very fine grits and wet chemicals as well as pad designs has been evolved to both remove and smooth the glass surface. That is, chemical polishing has heavily augmented pure mechanical polishing. Other materials besides glass, such as Al2O3, have also been polished to a high flatness for use in the magnetic disc head industry. Hence, the entry of CMP into the silicon IC industry was a path well traveled elsewhere.

The schematic of the CMP equipment is shown in Figures 1.9 and 1.10. This

Table 1.2: Comparison of spin on glass etchback and chemical mechanical polishing planarization.

	SOG Etchback	CMP
Planarization	Local (<10 μm)	Global (~10 mm)
Ability to prevent metal shorts	Variable	Good
Ability to meet depth-of-focus requirements	Poor (global topo > metal thickness)	Good (global topo ~ 1000-2000 Å)

polishing of glass surfaces is hundreds of years old in the optics business, but "new" to the IC process because it was originally considered too "dirty" to take wafers from dry process chambers into a wet polish slurry. The CMP process employs an automated rotating polishing platen and a wafer holder or chuck which sets the absolute planarity. The chuck can both exert a force on the wafer and simultaneously rotate the wafer independent of the rotation of the underlying platen. In between the wafer and the platen, the wafer polishing is accomplished by a polishing slurry consisting of colloidal silica (SiO_2) suspended in a KOH or other solution. An automatic slurry feeding system is used to ensure the uniform wetting of the polishing pad and the proper delivery and recovery of polishing slurry. For a unit designed for industrial use, automatic wafer loading and a cassette-to-cassette handler are also incorporated as well as post CMP cleaning.

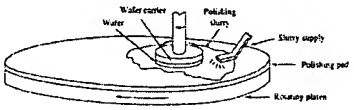

Figure 1.9: A schematic of a CMP polisher.

Planarization via polishing occurs when the polishing rate of "high" or protruding areas of the non-uniform topoligy is greater than the polishing rate in "low" or recessed areas. Is this planarization approach primarily a chemical or a mechanical process? We show below

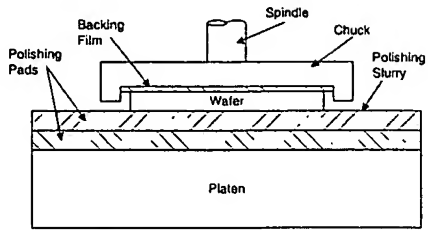

Figure 1.10: Detailed schematic of a CMP polisher. CMP uses "old" optics lap and polish methods.

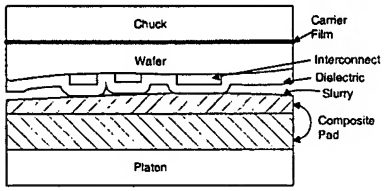

Figure 1.11: Cross-section of polishing technology employed in CMP.

it is both. The original oxide surface is reduced to $SiOH_x$ hydroxides by the KOH solution. Soft hydroxides are removed by abrasive action of colloidal SiO_2. The slurry of K-OH or ammonium hydroxide attacks the fresh oxide surface, forming new soft $SiOH_x$ complexes which are then removed.

The basic polishing mechanism for a SiO_2 dielectric is the same as for glass polishing in precision optics.

The mechanical removal rate of the glass is given by the Preston equation:

$$R = K_p p v$$

where: R = rate of removal in microns/min, p = pressure applied to wafer by polish pad in dynes/cm^2, v = relative velocity between the wafer and the polishing pad in cm/sec and K_p = proportionality constant called Preston's constant.

K_p has units of (pressure)$^{-1}$ and is known as the Preston coefficient. K_p is a function of:

- choice of materials to be polished flat, pad material and relative hardness of the pad, type of slurry particles, pH and concentration of slurry, and temperature [affects lot-to-lot uniformity].

- pad condition [affects wafer-to-wafer uniformity].
- material removal efficiency [along with pressure, affects within-wafer uniformity].

1.3.2 Mechanical Polishing Removal

In the same way that dry plasma etching of silicon requires both a chemical etch component (e.g. F atoms) and a physical etch component (e.g. F^+ ions), CMP requires both a chemical process and a mechanical process. The mechanical part of the process in effect physically sands down a thick primer layer to achieve a flat surface despite bumps/pits on the original surface. We will look at the chemical part of the process in the next section. Figure 1.12 and 1.13 shows dielectric oxide planarization and metal W planarization respectively using the pliable sanding pad in the CMP process.

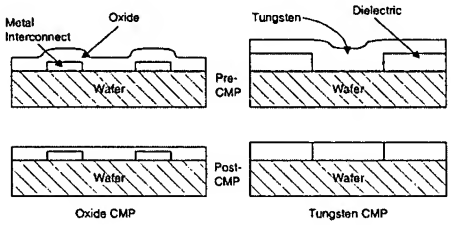

Figure 1.12: Pliable pad "sands" down the high-lying, non-planar topology.

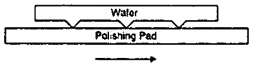

Figure 1.13: Close-up of "lap and polish" operation.

1.3.3 Pattern Sensitivity during CMP

Even the simple Preston's Law suggests that the polish rate will be dependent on underlying topography (i.e., pattern of poly or metal and other films):

$$\text{Removal rate} = K_p P v$$

where K_p = Preston's constant, P = applied pressure and v = relative velocity, because P (lbs/in^2) = F/A, where F = applied force, A = area being polished.

If applied force is kept constant, but the area being polished is varied (location dependent pattern density variations), then pad pressure will vary and so will removal rate. Hence the high lying features will be removed faster due to higher pressure in those local areas.

Further complications are added by pad deformation, slurry behavior, etc. — "total area" is not the only important factor. In summary, how the non-planar topography is broken up (many small areas vs. few large areas) will determine how we polish at different rates.

This change in removal rate with changing area of high-lying topology makes for a self-controlled soft landing when all high-lying topology is removed.

1.3.4 CMP Consumables

Like etch processes, CMP is critically dependent on chemical/physical feedstocks. For CMP, this involves the wet polishing slurry and associated consumables below:

- Slurry
- Backing film between chuck and wafer
- Final polish pad on wafer as well as polish pad on platen

Lots of money is required to replenish the above, in order to guarantee polished surfaces to ±200Å over 30 cm in diameter.

Changes in the slurry are also evolving. For example, NH_4OH-based slurry is replacing KOH-based slurry for dielectric polishing.

1.4 Chemical Removal of Film

1.4.1 CMP of Silicon

One chemical sequence of substrate dissolution and removal into the solvent during CMP is given in Figure 1.14. This wet surface chemistry aids the mechanical/physical grinding action of a silicon surface as shown. First, OH bonds to surface Si in the slurry particle. Second, OH attaches to the Si surface. This

Table 1.3: Comparison of KOH- and NH_4OH-based CMP processes.

Parameter	KOH-based	NH_4OH-based
Na conc. (ppb)	3200	10
K conc. (ppb)	Very high	100
Scratch density (norm)	5.5	0.8
Polish rate (Å/min)	1860	2160
Uniformity (% sigma)	4.1	4.8
Oxide surface roughness (Å)	288	32

weakens the back bond Si-Si attachment of the Si atom to the surface as follows. A second OH from the slurry attacks the H-O back bond. Finally, the Si-O-Si bond to the slurry particle is stronger than the Si-Si bond to the surface and this allows removal of the weakened silicon atom from the surface to be polished by the slurry.

CMP is clearly an emerging art, not yet a science due to its complexity. The art of CMP is partly in the firmness of the scouring or sanding pad as shown in Figure 1.15(a) and 1.15(b) for "soft" and "hard" pads, respectively. Hard pads with proper surface soft pressure yield good planarity. Conversely uniformity requires a soft pad and high pressure to conform to variations of the wafer surface. A wafer can be planar but not uniform and vice-versa. A compromise is a hard outer pad with an underlying soft pad.

1.4.2 CMP of Metal

Metal CMP, in contrast to SiO_2 CMP, relies on the fact that we can continuously grow oxide on metal everywhere by oxidant wet chemistry. The oxide of metal has 100 times lower etch rate than the pure metal. We remove only high lying metal in the CMP process because only there do we physically remove the protective oxide. Then wet chemistry dissolves the exposed high-lying metal. If the slurry contains sufficient oxidants, removal of oxide by the pad is followed by regrowth of oxide. This sequence is shown below in Figure 1.16. We first form a thin oxide on all the surfaces. The fine mechanical scratching removes the high part of the metal oxide. The wet etchant then removes this exposed high metal but not the low metal covered by oxide. We repeat the process until we reach planar metal surfaces.

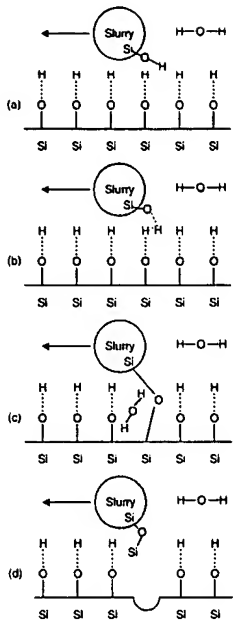

Figure 1.14: The mechanism of CMP: (a) In aqueous solution, oxide forms hydroxyls; (b) hydrogen bond is formed between the slurry particle and the wafer; (c) Si-O bonds are formed by releasing a water molecule; (d) the Si-Si bond breaks when the slurry particle moves away.

In the CMP removal of tungsten, the process is mostly a chemical process. Slurries used typically have one of three oxidizers: potassium iodate, hydrogen peroxide, or ferric nitrate. They are typically acidic solutions (PH = 1–4.5) and use alumina or silica abrasives. Again we need to properly balance the role of the oxidants (passivant) versus the acid (etchant). The abrasives act only on high-lying surfaces. The mechanism of oxidation followed by abrasion/removal of the surface oxide followed by re-oxidation is the CMP process for tungsten.

There are various W polish slurries available commercially with different combinations of oxidizers and abrasives. Some oxidizers tend to be more aggressive and can cause recessed plugs and plug "coring", while others from more passivating oxides and are less susceptible to this problem. Some slurries cause significant damage (pits, dings, and scratches) to the oxide layer (typically slurries with alumina abrasive) after the tungsten clears. An oxide layer buff cycle with oxide slurry is then required to repair surface oxide.

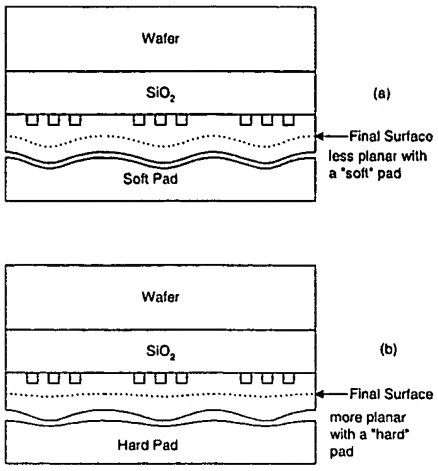

Figure 1.15: The difference in final surface planarization with soft and hard pads.

The range of planarization achieved using CMP and various other methods is reviewed in Figure 1.17 using the definitions of both R and θ from Figure 1.6. An IC high rise cross-section made without CMP and with CMP is shown in Figure 1.18. Clearly CMP brings a tidy regimented planar look to the entire IC and many of the photolithography, dry etch, and metalization problems with non-planar topology are removed. Hence IC yield increases and the extra CMP steps required actually pay for themselves.

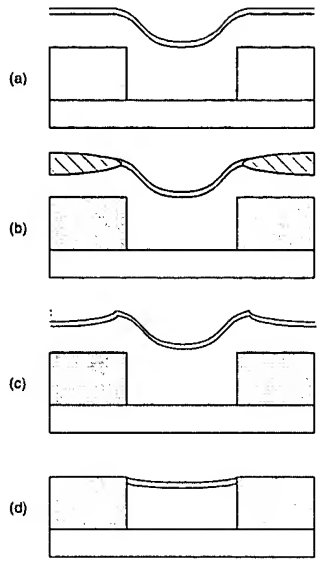

Figure 1.16: Mechanism for metal polishing: (a) Free metal surface is covered by a passivation oxide; (b) the oxide on the high spots is removed by CMP and the metal is etched by the solution (cross-hatched area); (c) regrowth of oxide; (d) process in (b) and (c) repeat until no high spot is left.

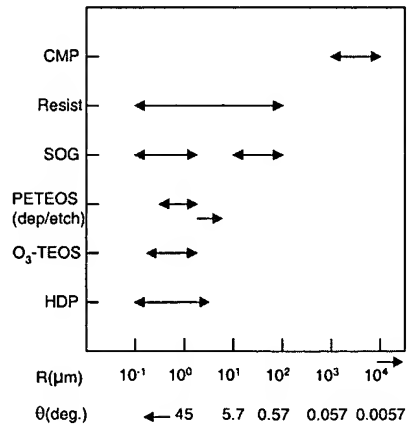

Figure 1.17: The range of planarization for various processes. Recall from Figure 1.7 that large R and small θ indicate planar surfaces.

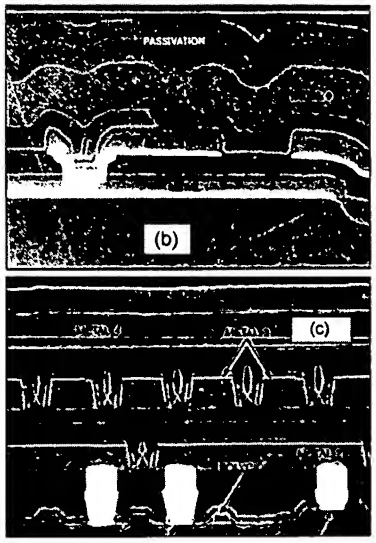

Figure 1.18: SEM's show (b) a three-metal layer device without CMP and (c) a four-metal layer microprocessor using CMP. (Source: Integrated Circuit Engineering Corp.)

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